AMENDMENTS TO THE CLAIMS

In the Claims:

Please amend claims 1-2, 4 and 6-7 as follows:

Claim 1. (Currently Amended) A method for manufacturing multi-level interconnection lines of a semiconductor device comprising:

forming a first interconnection line in a second interlayer insulating layer and a first etching stop layer sequentially formed on a first interlayer insulating layer disposed on a semiconductor substrate;

forming a third interlayer insulating layer on the first interconnection line and the first etching stop layer;

forming a second etching stop layer on the third interlayer insulating layer;

forming a via hole exposing the first interconnection line by selectively etching the second etching stop layer and the third interlayer insulating layer;

forming an etching stop pattern around an inlet of the via hole by selectively etching the second etching stop layer leaving a portion of the second etching stop layer around the inlet of the via hole and exposing a portion of the third interlayer insulating layer;

forming a fourth interlayer insulating layer on the portion of the second etching stop layer disposed around the inlet of the via hole and the exposed portion of the third interlayer insulating layer and at least partially covering the via hole;

forming a trench by selectively etching the fourth interlayer insulating layer to expose the portion of the second etching stop layer disposed around the via hole; and

forming a conductive layer in the trench and in the via hole so that the conductive layer at least partially covers the portion of the second etching stop layer disposed around the inlet of the via hole.

Claim 2. (Previously Presented) The method of claim 1, wherein the method further comprises:

forming a photoresist pattern around the inlet of the via hole to cover the portion of the second etching stop layer disposed around the inlet of the via hole; and

removing other portions of the second etching stop layer which are not covered with the photoresist pattern to expose the portion of the third interlayer insulating layer.

Claim 3. (Canceled).

Claim 4. (Previously Presented). The method of claim 1, wherein the trench exposes part of the portion of the second etching stop layer disposed around the via hole.

Claim 5. (Previously Presented). The method of claim 1, wherein the width of the trench is wider than that of the via hole.

Claim 6. (Previously Presented). The method of claim 1, wherein a void is formed in the fourth interlayer insulating layer during the step of forming the fourth interlayer insulating layer.

Claim 7. (Currently Amended). The method of claim 6, wherein the fourth interlayer insulating layer is formed with any one selected from the group consisting of an USG layer deposited by a high density plasma[[,]] and an oxide deposited either

by plasma enhanced chemical vapor deposition or low pressure chemical vapor deposition.

Claim 8. (Previously Presented) The method of claim 6, wherein the fourth interlayer insulating layer is formed at a thickness ranging from about 2000 Å to about 30000 Å.

Claim 9. (Previously Presented). The method of claim 1, wherein the first to third interlayer insulating layers are formed with any one selected from the group consisting of a spin on glass layer, an oxide layer deposited by a plasma enhanced chemical vapor deposition method, an oxide layer deposited by a high density plasma method and a tetra-ethyl-ortho-silicate(TEOS) layer.

Claim 10. (Previously Presented). The method of claim 9, wherein the first to third interlayer insulating layers are formed at a thickness ranging from about 3000 Å to about 30000 Å.

Claim 11. (Previously Presented) The method of claim 1, wherein the second etching stop layer is formed with any one selected from the group consisted of a nitride layer deposited by a plasma enhanced chemical vapor deposition method, a SiON layer, a Ta_2O_5 layer, a ZnO_2 layer, a ZrO_2 layer, a ZnO layer, a HfO layer and an Al_2O_3 layer.

Claim 12. (Previously Presented). The method of claim 11, wherein the second etching stop layer is formed at a thickness ranging from about 200 Å to about 3000 Å.

Claim 13. (Original). The method of claim 1, wherein the first interconnection line is formed of any one selected form a group consisting of Al, Cu, Au, Ag and Cr.

Claim 14. (Original). The method of claim 1, the first interconnection line is formed at a thickness ranging from about 2000 Å to about 30000 Å.

Claims 15-20. (Canceled).